
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: PRITCHARD et al.

Attorney Docket No.:
03-2051/LSIIP240

Application No.: 10/791,337

Examiner: TRINH, Michael M.

Filed: March 1, 2004

Group: 2822

Title: SPACER-LESS TRANSISTOR
INTEGRATION SCHEME FOR HIGH-K GATE
DIELECTRICS AND SMALL GATE-TO-GATE
SPACES APPLICABLE TO SI, SIGE AND
STRAINED SILICON SCHEMES

Confirmation No.: 2401

CERTIFICATE OF EFS-WEB TRANSMISSION

I hereby certify that this correspondence is being transmitted electronically
through EFS-WEB to the Commissioner for Patents, P.O. Box 1450, Alexandria,
VA 22313-1450 on June 6, 2007.

Signed:


Sue Funchess

AMENDMENT C

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Office Action dated April 4, 2007, please amend the above-identified
patent application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this
paper.

Remarks/Arguments begin on page 5 of this paper.